



FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>		ATTY. DOCKET NO. 0077.20 (1778.0120002)		APPLICATION NO. 09/364,786	
		APPLICANT Thekkath et al.			
		FILING DATE July 30, 1999		GROUP 2672	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
D7L	AA1	4,866,652	09/1989	Chu et al.			
D7L	AB1	5,025,407	06/1991	Gulley et al.			
D7L	AC1	5,159,665	10/1992	Priem et al.			
D7L	AD1	5,206,823	04/1993	Hesson			
D7L	AE1	5,220,524	06/1993	Hesson			
D7L	AF1	5,257,216	10/1993	Sweedler			
D7L	AG1	5,278,949	01/1994	Thayer			
D7L	AH1	5,341,321	08/1994	Karp et al.			
D7L	AI1	5,367,650	11/1994	Sharangpani et al.			
D7L	AJ1	5,420,966	05/1995	Silverbrook			
D7L	AK1	5,420,971	05/1995	Westerink et al.			

FOREIGN PATENT DOCUMENTS

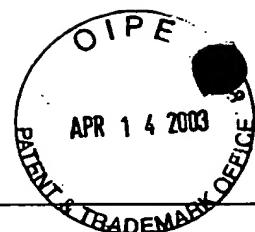
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

D7L	AR	1	Higaki, N. et al., "A 2.5 GFLOPS 6.5 Million Polygons per Second 4-Way VLIW Geometry Processor with SIMD Instructions and a Software Bypass Mechanism," 1999 IEEE International Solid-State Circuits Conference, IEEE, 11 pages (publication date unknown, conference dates: February 15-17, 1999).
D7L	AS	1	Hughes, J.K., <i>PL/I Programming</i> , John Wiley & Sons, pp. 5, 15, 16, 74, 75, 188, 189, 327, 411-416, 423, 424, 689 and 690 (1973).
D7L	AT	1	Ito, M. et al., "Efficient Initial Approximation for Multiplicative Division and Square Root by a Multiplication with Operand Modification," <i>IEEE Transactions on Computers</i> , IEEE, Vol. 46, No. 4, pp. 495-498 (April 1997).

EXAMINER	Daniel Chung	DATE CONSIDERED	6/28/01
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
D7C	AA2	5,530,663	06/1996	Garcia et al.			
D7C	AB2	5,805,486	09/1998	Sharangpani			
D7C	AC2	5,847,979	12/1998	Wong et al.			
D7C	AD2	5,880,983	03/1999	Elliott et al.			
D7C	AE2	5,889,690	03/1999	Arakawa			
D7C	AF2	5,892,698	04/1999	Naffziger			
D7C	AG2	5,923,577	07/1999	Wong et al.			10/21/1996
D7C	AH2	5,928,316	07/1999	Wong et al.			11/18/1996
D7C	AI2	5,999,960	12/1999	Gerwig et al.			12/16/1996
D7C	AJ2	6,169,554 B1	01/2001	Deering			06/30/1997
D7C	AK2	6,175,370 B1	01/2001	Kunimatsu			01/31/1997

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

D7C	AR	2	Kubosawa, H. et al., "A 2.5-GFLOPS, 6.5 Million Polygons per Second, Four-Way VLIW Geometry Processor with SIMD Instructions and a Software Bypass Mechanism," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 11, pp. 1619-1626 (November 1999) (appears to correspond to document AR1, Hikagi, N. et al.).
D7C	AS	2	"MIPS Extension for Digital Media with 3D," MIPS Technologies, Inc., pages 1-26 (March 1997).
D7C	AT	2	"MIPS IV Instruction Set," Revision 3.2, MIPS Technologies, Inc., pages B-21, B-22, B-26, B-28, B-38, B-39, B-40, B-41, B-42, B-47, B-48, B-49, B-55, B-95, B-96 (September 1995).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
DX	AA3	6,249,798 B1	06/2001	Golliver et al.			10/10/1996
DZC	AB3	6,275,838 B1	08/2001	Blomgren et al.			10/28/1998
DZC	AC3	6,426,746 B2	07/2002	Hsieh et al.			03/31/1998
DZC	AD3	4,839,846	06/1989	Hirose et al.			
DZC	AE3	5,038,313	08/1991	Kojima			
DZC	AF3	5,511,016	04/1996	Béchade			
DZC	AG3	5,550,767	08/1996	Taborn et al.			
DZC	AH3	5,553,015	09/1996	Elliott et al.			
DZC	AI3	5,602,769	02/1997	Yu et al.			
DZC	AJ3	6,199,089 B1	03/2001	Mansingh			09/18/1998
DZC	AK3	6,510,446 B1	01/2003	Fukagawa			11/22/1999

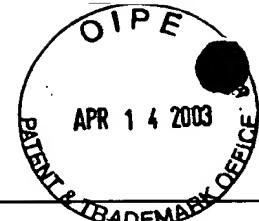
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DZC	AR	3	"MIPS V Instruction Set," Revision 1.0, MIPS Technologies, Inc., pages B-1 - B-37 (1996).
DZC	AS	3	Sweetman, D., See MIPS Run, Morgan Kaufmann Publishers, Inc., ISBN 1-55860-410-3, pp. vii-xiv, 149-173, and 201-242 (1999).
	AT	3	

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D7C	AA4	5,631,859	05/1997	Markstein et al.			
D7C	AB4	5,652,875	07/1997	Taylor			
D7C	AC4	5,671,170	09/1997	Markstein et al.			
D7C	AD4	5,701,442	12/1997	Ronen			
D7C	AE4	5,768,170	06/1998	Smith			
D7C	AF4	5,995,122	11/1999	Hsieh et al.			04/30/1998
D7C	AG4	5,996,066	11/1999	Yung			10/10/1996
AH4							
AI4							
AJ4							
AK4							

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	4	
	AS	4	
	AT	4	

EXAMINER

Daniel chung

DATE CONSIDERED

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